

**Patent**

Customer No. 31561  
Docket No. 11417-US-PA  
Application No.: 10/707,358

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of

Applicant : Wang  
Application No. : 10/707,358  
Filed : Dec. 8, 2003  
For : SEMICONDUCTOR DEVICE AND FABRICATING  
METHOD THEREOF  
Examiner : N/A  
Art Unit : 2811

**INFORMATION DISCLOSURE STATEMENT**

ASSISTANT COMMISSIONER FOR PATENTS  
Arlington, VA 22202

Enclosed is a PTO Form 1449 listing 1 reference(s), copy of which is attached. Applicant submits the reference(s) in compliance with his duty of disclosure pursuant to 37 CFR § 1.56 and 1.97. The Examiner is requested to make the citation(s) of official record.

This IDS is being submitted before the first Office Action. Thus, it is believed no fee is due.

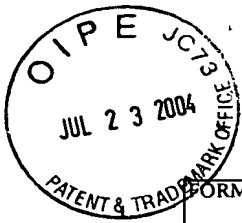
The submission of the reference(s) should not be interpreted as admitting them as prior art.

Respectfully Submitted,  
JIANQ CHYUN Intellectual Property Office

Date: July 21, 2004

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICATION	ATTY. DOCKET NO.: 11417-US-PA	APPLICATION NO.: 10/707,358
	APPLICANT: Wang	
	FILING DATE: Dec. 8, 2003	GROUP 2811

#### U.S. PATENT DOUCMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FIILNG DATE (IF APPROPRIATE)

#### FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	FIILNG DATE (IF APPROPRIATE)

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
C.L.	Chuang, D. R., <i>VLSI Process Technology</i> , 1997/2/15, p.404, Figure 11-9.

EXAMINER	DATE CONSIDERED
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EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEST COMMUNICATION TO APPLICANT.